

Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Canceled)
2. (Previously Presented) The semiconductor device as set forth in claim 32, wherein said electrically insulating film contains one of Hf and Zr.
3. (Previously Presented) The semiconductor device as set forth in claim 32, further comprising a layer containing one of Hf and Zr therein between said electrically insulating film and said gate electrode.
4. (Previously Presented) The semiconductor device as set forth in claim 32, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and one of a Hf-containing layer and a Zr-containing layer.
5. (Previously Presented) The semiconductor device as set forth in claim 32, wherein said electrically insulating film contains HfSiON.
6. (Previously Presented) The semiconductor device as set forth in claim 32, further comprising a HfSiON layer between said electrically insulating film and said gate electrode.
7. (Previously Presented) The semiconductor device as set forth in claim 32, wherein said electrically insulating film has a multi-layered structure including one of a silicon oxide film and a silicon nitride film, and a HfSiON layer.
- 8-9. (Canceled)

1 10. (Currently Amended) The semiconductor device as set forth in claim 32,
2 wherein, said gate electrode contains nickel silicide as a primary constituent,
3 and assuming that a region of said nickel silicide (~~including nickel (Ni) as said~~
4 ~~metal-M~~) making contact with said gate insulating film is expressed with
5 $\text{Ni}_x\text{Si}_{1-x}$ ($0 < X < 1$), said X is equal to or greater than 0.6 and smaller
6 than 1 ($0.6 \leq X < 1$) in said nickel silicide contained in a gate electrode formed
7 above a p-channel, and said X is greater than 0 and equal to or smaller than
8 0.5 ($0 < X \leq 0.5$) in said nickel silicide contained in a gate electrode formed
9 above a n-channel.

1 11. (Currently Amended) The semiconductor device as set forth in claim 32,
2 wherein said nickel silicide contained in said gate electrode formed above said
3 p-channel contains Ni_3Si Ni_3Si phase as a principal constituent at least in a
4 region through which said nickel silicide makes contact with said gate
5 insulating film, and said nickel silicide contained in said gate electrode formed
6 above said n-channel contains one of NiSi phase and NiSi_2 NiSi_2 phase as a
7 principal constituent at least in a region through which said nickel silicide
8 makes contact with said gate insulating film.

1 12. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film,
4 wherein at least a region of said gate electrode making contact with
5 said gate insulating film is composed of silicide containing Ni_3Si phase as a
6 principal constituent.

1 13. (Original) The semiconductor device as set forth in claim 12, wherein said
2 gate insulating film includes an electrically insulating film having a high
3 dielectric constant and containing one of metal oxide, metal silicate and metal
4 oxide or metal silicate containing nitrogen therein,

1 14. (Original) The semiconductor device as set forth in claim 13, wherein said
2 electrically insulating film contains one of Hf and Zr.

1 15. (Original) The semiconductor device as set forth in claim 13, further
2 comprising a layer containing one of Hf and Zr therein between said
3 electrically insulating film and said gate electrode.

1 16. (Original) The semiconductor device as set forth in claim 13, wherein said
2 electrically insulating film has a multi-layered structure including one of a
3 silicon oxide film and a silicon nitride film, and one of a Hf-containing layer
4 and a Zr-containing layer.

1 17. (Original) The semiconductor device as set forth in claim 13, wherein said
2 electrically insulating film contains HfSiON.

1 18. (Original) The semiconductor device as set forth in claim 13, further
2 comprising a HfSiON layer between said electrically insulating film and said
3 gate electrode.

1 19. (Original) The semiconductor device as set forth in claim 13, wherein said
2 electrically insulating film has a multi-layered structure including one of a
3 silicon oxide film and a silicon nitride film, and a HfSiON layer.

1 20. (Previously Presented) The semiconductor device as set forth in claim 12,
2 wherein said gate electrode is included in a p-type MOSFET.

1 21. (Previously Presented) A method of fabricating a semiconductor device,
2 comprising:
3 depositing poly-silicon (poly-Si) on a gate insulating film and

4 patterning said poly-silicon into a gate electrode having desired dimension;
5 depositing one of metals selected from Ni, Pt, Ta, Ti, Hf, Co, Zr and V
6 on said gate electrode;
7 thermally annealing said gate electrode and said one of metals to
8 entirely turn said gate electrode to silicide of said one of metals; and
9 removing a portion of said one of metals which was not turned into
10 said silicide, by etching,
11 assuming that said one of metals is expressed with M, and said silicide
12 has a portion through which said silicide makes contact with said gate
13 insulating film and which has a composition expressed with M_xSi_{1-x} (0<X<1),
14 wherein said metal M has such a thickness t1 above a p-channel device
15 that, when poly-silicon and said metal M react with each other to make
16 silicide, a portion of said silicide making contact with said gate insulating film
17 has composition expressed with M_xSi_{1-x} (0.5<X<1), and has such a thickness
18 t2 above a n-channel device that, when poly-silicon and said metal M react
19 with each other to make silicide, a portion of said silicide making contact with
20 said gate insulating film has composition expressed with M_xSi_{1-x} (0<X≤0.5).

1 22. (Previously Presented) A method of fabricating a semiconductor device,
2 comprising:
3 depositing poly-silicon on a gate insulating film and patterning said
4 poly-silicon into a gate electrode having desired dimension;
5 forming a nickel (Ni) film on said gate electrode;
6 thermally annealing said gate electrode and said nickel film to entirely
7 turn said gate electrode to nickel silicide (NiSi); and
8 removing a portion of said nickel film which was not turned into said
9 nickel silicide, by etching,
10 wherein said nickel film has such a thickness t1 above a p-channel
11 device that, when poly-silicon and nickel react with each other to make nickel
12 silicide, a portion of said nickel silicide making contact with said gate

13 insulating film has composition expressed with Ni_xSi_{1-x} ($0.6 \leq X < 1$), and has
14 such a thickness t_2 above a n-channel device that, when poly-silicon and
15 nickel react with each other to make nickel silicide, a portion of said nickel
16 silicide making contact with said gate insulating film has composition
17 expressed with Ni_xSi_{1-x} ($0 < X \leq 0.5$).

1 23. (Previously Presented) A method of fabricating a semiconductor device,
2 comprising:

3 depositing poly-silicon on a gate insulating film and patterning said
4 poly-silicon into a gate electrode having desired dimension;
5 forming a nickel (Ni) film on said gate electrode;
6 thermally annealing said gate electrode and said nickel film to entirely
7 turn said gate electrode to nickel silicide (NiSi); and
8 removing a portion of said nickel film which was not turned into said
9 nickel silicide, by etching,

10 wherein said nickel film has such a thickness t_1 above a p-channel
11 device that, when poly-silicon and nickel react with each other to make nickel
12 silicide, said nickel silicide has Ni_3Si phase as a principal constituent, and has
13 such a thickness t_2 above a n-channel device that, when poly-silicon and
14 nickel react with each other to make nickel silicide, said nickel silicide has one
15 of $NiSi$ phase and $NiSi_2$ phase as a principal constituent.

1 24. (Original) The method as set forth in claim 23, wherein a ratio of a
2 thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is
3 defined as $T_{Ni}/T_{Si} \geq 1.60$ to form said gate electrode including Ni_3Si phase as a
4 principal constituent.

1 25. (Original) The method as set forth in claim 23, wherein a ratio of a
2 thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is
3 defined as $0.55 \leq T_{Ni}/T_{Si} \leq 0.95$ to form said gate electrode including $NiSi$

4 phase as a principal constituent.

1 26. (Original) The method as set forth in claim 23, wherein a ratio of a
2 thickness T_{Ni} of said nickel film to a thickness T_{Si} of said poly-silicon is
3 defined as $0.28 \leq T_{Ni}/T_{Si} \leq 0.54$, and said gate electrode and said nickel film
4 are thermally annealed at 650 degrees centigrade or higher to form said gate
5 electrode including $NiSi_2$ phase as a principal constituent.

1 27. (Currently Amended) The method as set forth in claim 26 21, wherein the
2 step of depositing said metal M or forming said nickel film comprises:
3 after forming said metal M or said nickel film above a n-channel
4 device or a p-channel device by the thickness of t2, forming
5 diffusion-preventing layer which is stable to said metal M or nickel, only
6 above said n-channel device; and
7 depositing said metal M or forming said nickel film by the thickness of
8 (t1 – t2).

1 28. (Original) The method as set forth in claim 27, wherein said
2 diffusion-preventing layer can be etched in selected areas relative to silicide of
3 said metal M.

1 29. (Original) The method as set forth in claim 27, wherein said
2 diffusion-preventing layer contains one of TiN and TaN as a primary
3 constituent.

1 30. (Currently Amended) The method as set forth in claim 26 21, wherein said
2 gate electrode and said metal M or said nickel film are thermally annealed for
3 silicidation at such a temperature that a resistance of metal silicide formed in a
4 diffusion contact region of said semiconductor device is not increased.

1 31. (Currently Amended) A method of fabricating a semiconductor device,
2 comprising:
3 depositing poly-silicon on a gate insulating film and patterning said
4 poly-silicon into a gate electrode having desired dimension;
5 forming a nickel (Ni) film on said gate electrode;
6 thermally annealing said gate electrode and said nickel film to entirely
7 turn said gate electrode to nickel silicide (NiSi); and
8 removing a portion of said nickel film which was not turned into said
9 nickel silicide, by etching,
10 wherein a ratio of a thickness T_{Ni}/T_{Si} of said nickel film to a thickness
11 T_{Si}/T_{Si} of said poly-silicon is defined as $1.60 \leq T_{Ni}/T_{Si} \leq T_{Si}/T_{Si}$.

1 32. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,
4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,
7 said gate electrode contains nickel silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with Ni_xSi_{1-x}
10 ($0 < x < 1$), and
11 said X is greater than 0.5 ($X > 0.5$) in said nickel silicide contained in a
12 gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said nickel silicide contained in a gate electrode formed
14 above a n-channel.

1 33. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains platinum silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with $\text{Pt}_x\text{Si}_{1-x}$
10 ($0 < X < 1$), and

11 said X is greater than 0.5 ($X > 0.5$) in said platinum silicide contained in
12 a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said platinum silicide contained in a gate electrode formed
14 above a n-channel.

1 34. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains tantalum silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with $\text{Ta}_x\text{Si}_{1-x}$
10 ($0 < X < 1$), and

11 said X is greater than 0.5 ($X > 0.5$) in said tantalum silicide contained in
12 a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said tantalum silicide contained in a gate electrode formed
14 above a n-channel.

1 35. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains titanium silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with Ti_xSi_{1-x}
10 ($0 < X < 1$), and

11 said X is greater than 0.5 ($X > 0.5$) in said titanium silicide contained in
12 a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said titanium silicide contained in a gate electrode formed
14 above a n-channel.

1 36. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains hafnium silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with Hf_xSi_{1-x}
10 ($0 < X < 1$), and

11 said X is greater than 0.5 ($X > 0.5$) in said hafnium silicide contained in
12 a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said hafnium silicide contained in a gate electrode formed
14 above a n-channel.

1 37. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains cobalt silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with
10 $\text{Co}_x\text{Si}_{1-x}$ (0 < X < 1), and

11 said X is greater than 0.5 (X > 0.5) in said cobalt silicide contained in a
12 gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 (X ≤ 0.5) in said cobalt silicide contained in a gate electrode formed
14 above a n-channel.

1 38. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains zirconium silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with $\text{Zr}_x\text{Si}_{1-x}$
10 (0 < X < 1), and

11 said X is greater than 0.5 (X > 0.5) in said zirconium silicide contained
12 in a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 (X ≤ 0.5) in said cobalt zirconium contained in a gate electrode formed
14 above a n-channel.

1 39. (Previously Presented) A semiconductor device comprising a silicon
2 substrate, a gate insulating film formed on said silicon substrate, and a gate
3 electrode formed on said gate insulating film, in this order,

4 wherein said gate insulating film includes an electrically insulating
5 film having a high dielectric constant and containing one of metal oxide, metal
6 silicate and metal oxide or metal silicate containing nitrogen therein,

7 said gate electrode contains vanadium silicide as a primary constituent,
8 and has a region through which said gate electrode makes contact with said
9 gate insulating film and which has a composition expressed with V_xSi_{1-x}
10 ($0 < X < 1$), and

11 said X is greater than 0.5 ($X > 0.5$) in said vanadium silicide contained
12 in a gate electrode formed above a p-channel, and said X is equal to or smaller
13 than 0.5 ($X \leq 0.5$) in said cobalt vanadium contained in a gate electrode formed
14 above a n-channel.